REMARKS

At the time of the Office Action dated February 6, 2008, claims 1 and 3-8 were pending in this application. In this Amendment, claims 1, 3, and 4 have been amended, and new claim 9 added. Care has been exercised to avoid the introduction of new matter. Support for the present Amendment can be found in, for example, Figs. 2, 3, and 6 and relevant description of the specification.

Claims 1 and 3-9 are now active in this application, of which claim 1 is independent.

Claims 1 and 3-8 have been rejected under 35 U.S.C. §103(a) as being unpatentable over Ganapathy et al. in view of Levenstein.

In the statement of the rejection, the Examiner asserted that the applied combination of Ganapathy et al. and Levenstein teaches the claimed subject matter. Applicant submits that Ganapathy et al. and Levenstein, either individually or in combination, do not disclose or suggest a direct memory access controller including all the limitations recited in independent claim 1. Specifically, the applied combination does not teach, among other things, "said control portion permits transferring to a first portion of said direct memory access transfer portions based on values set in said first group, and permits transferring to a second portion of said direct memory access transfer portions based on values set in said second group after transferring by said first portion, in one granting period of transferring by the arbiter," as recited in claim 1.

The direct memory access controller is coupled with the arbiter which arbitrates the bus right between the direct memory access controller and another circuit such as a central processing unit. The direct memory access controller includes a plurality of direct memory access transfer portions, the control portion, and the two groups of registers. The control portion

permits one of the plural direct memory access transfer portions to perform transferring, and then permits another of the plural direct memory access transfer portions to perform transferring, in the granted period of the arbiter. In other words, the control portion can change from data transfer by the first direct memory access transfer portion to data transfer by the second direct memory access transfer portion while the arbiter allows the direct memory access controller to use the bus.

Ganapathy et al. discloses an apparatus for distributed direct memory access. A bus multiplexes a number of DMA transactions at one time, and one transaction of the DMA is dealt at a time. Ganapathy et al. does not teach the direct memory access controller which performs plural data transfer transactions in one granting period by the bus arbiter. Nor does Levenstein teach performing plural data transfer transactions in one granting period by the bus arbiter.

Based on the foregoing, Applicant submits that Ganapathy et al. and Levenstein, either individually or in combination, do not disclose or suggest a direct memory access controller including all the limitations recited in independent claim 1. Dependent claims 3-8 are also patentably distinguishable over Ganapathy et al. and Levenstein at least because these claims respectively include all the limitations recited in independent claim 1. Applicant, therefore, respectfully solicits withdrawal of the rejection of the claims and favorable consideration thereof.

New Claim 9

Applicant submits that new claim 9 are patentably distinguishable over Ganapathy et al. and Levenstein at least because the claim includes all the limitations recited in independent claim 1. Favorable consideration is respectively solicited.

Conclusion

It should, therefore, be apparent that the imposed rejections have been overcome and that all pending claims are in condition for immediate allowance. Favorable consideration is, therefore, respectfully solicited.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

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